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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,019	06/22/2005	Hiroshi Iwata	0020-5383PUS1	8857

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EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
08/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/540,019	IWATA ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *7,8,18,19,21,22,24-26 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-17,20,23,27 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The amendment after final dated 07/08/08 has been entered.

Rejections and/or objections necessitated by the amendments dated 01/03/08

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6, 9, 10, 11, 13, 16, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (US pub 20060208312).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 1, Iwata et al. teach a semiconductor storage device comprising (see fig. 2 and associated text):

a semiconductor layer 1;

a gate conductor 3 formed on the semiconductor layer, said gate conductor consisting of a single gate electrode formed on the semiconductor layer with a gate insulation film 2 disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions 13a, 13b arranged on opposite sides of the channel region; and memory function bodies 11a,11b formed on opposite sides of the gate electrode and having a function to retain electric charges, wherein gate conductor functions for writing to, and erasing and reading from the semiconductor storage device are solely carried out with the single gate electrode (see paragraphs [0436] and [0587]).

With respect to claim 6, Iwata et al. further teach each of the memory function bodies is comprised of one or more insulative materials 16,12 and at least part of each memory function body is formed so as to overlap with part of the corresponding diffusion region.

With respect to claim 9, Iwata et al. further teach wherein each of the memory function bodies includes a charge retention film 17 having a function of storing electric charges, and an insulator 16 or 12.

With respect to claim 10, Iwata et al. further teach wherein the charge retention film includes a first portion that has a surface roughly parallel to a surface of the gate insulation film.

With respect to claim 11, Iwata et al. further teach wherein the charge retention film includes a second portion extended roughly parallel to a side surface of the gate electrode or the word line.

With respect to claim 12, Iwata et al. further teach wherein the insulator includes an insulation film 12 that separates the gate electrode or the word line from the second portion of the charge retention film extended roughly parallel to the side surface of the gate electrode or the word line.

With respect to claim 13, Iwata et al. further teach wherein the insulator includes an insulation film 12 that separates the first portion of the charge retention film from the channel region or the semiconductor layer.

With respect to claim 16, Iwata et al. further teach wherein each diffusion region is effectively offset with respect to the gate electrode.

With respect to claim 29, Iwata et al. further teach the gate electrode does not cover the memory function bodies.

Claims 2, 23, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (US 20060208312).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 2, Iwata et al. teach a semiconductor storage device comprising (see fig. 2 and associated text):

a semiconductor layer 1; a gate conductor 3 formed on the semiconductor layer, said gate conductor consisting of a single gate electrode 3 formed on the semiconductor layer with a gate insulation film 2 disposed therebetween;

a channel region arranged under the gate electrode;

diffusion regions 13a,13b arranged on opposite sides of the channel region; and

two charge storage regions 17, each of the charge storage regions being in a shape of a film parallel to a surface of the semiconductor layer and existing over part of the channel region and part of the corresponding diffusion region, straddling a boundary therebetween, wherein gate conductor functions for writing to, and erasing and reading from the semiconductor storage device are solely carried out with the single gate electrode.

With respect to claim 23, Iwata et al. further teach wherein each diffusion region is effectively offset with respect to the gate electrode.

With respect to claim 30, Iwata et al. further teach the gate electrode does not cover the charge storage regions.

Claims 3, 4, 5, 17, 27, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (US 20060208312).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 3, Iwata et al. teach a semiconductor storage device comprising (see fig. 2 and associated text):

a plurality of memory elements arranged along a word line,

wherein two memory function bodies 11a,11b having a function to retain electric charges are formed so as to extend along the word line on opposite sides of the word line 3,

each of the plurality of memory elements comprising:

a semiconductor layer 1 ;

a gate conductor 3 formed on the semiconductor layer, said gate conductor consisting of a single gate electrode 3 and comprising a part of the word line;

a gate insulation film 2 formed between the semiconductor layer and the part of the word line;

a channel region arranged under the part of the word line;

diffusion regions 13a,13b arranged on opposite sides of the channel region; and

a part of each of the memory function bodies that exists over part of the channel region and part of the corresponding diffusion region, straddling a boundary therebetween, wherein

gate conductor functions for writing to, and erasing and reading from each memory element are solely carried out with the single gate electrode.

With respect to claim 4, Iwata et al. further teach the word line consists of a single word line, the memory function bodies are arranged only on both sides of the

single word line, and the memory function bodies are each comprised of one or more insulative materials 16 or 12.

With respect to claim 5, Iwata et al. further teach a word line 3 to be selected when information is rewritten to the memory element is only the single word line. See fig. 2 and associated text.

With respect to claim 17, Iwata et al. further teach wherein each diffusion region is effectively offset with respect to the word line.

With respect to claim 27, Iwata et al. further teach wherein each of the memory function bodies includes a charge retention film 17 having a function of storing electric charges, and an insulator 16 or 12.

With respect to claim 31, Iwata et al. further teach the word line does not cover the memory function bodies.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. (US pub 20060208312).

With respect to claim 20, the use of flash memory device as flash drive ro portable electronic equipment is well-known in semiconductor device.

With respect to claim 14, Iwata et al. further teach the insulation film 12 or 16 that separates the first portion of the charge retention film from the channel region or the semiconductor layer has a film thickness but fails to teach the thickness of the insulation

film which is smaller than a film thickness of the gate insulation film and not smaller than 0.8 nm.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of the insulation film through routine experimentation and optimization to obtain optimal or desired device performance because the thickness of the insulation film is a result-effective variable and there is no evidence indicating that the thickness of the insulation film is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 15, Iwata et al. further teach the insulation film 12 or 16 that separates the first portion of the charge retention film from the channel region or the semiconductor layer has a film thickness but fails to teach the thickness of the insulation film which is smaller than a film thickness of the gate insulation film and not smaller than 20 nm.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the thickness of the insulation film through routine experimentation and optimization to obtain optimal or desired device performance because the thickness of the insulation film is a result-effective variable and there is no evidence indicating that the thickness of the insulation film is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 9-17, 20, 23, 27, and 29-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham

Primary Examiner
Art Unit 2814

/Long Pham/
Primary Examiner, Art Unit 2814